

CLAIMS

What is claimed is:

1. A method comprising:
 - determining if a predetermined limit of global functional activity in an integrated circuit has been met or exceeded;
 - and if so, then
 - reducing a high frequency of clocking of circuitry gradually to zero to stop the clocking of circuitry,
 - waiting a predetermined time after stopping the clocking of circuitry, and
 - starting the clocking of circuitry at a low frequency.
2. The method of claim 1, wherein if the determining if the predetermined limit of global functional activity in the integrated circuit has not been met or exceeded, it is repeated.
3. The method of claim 1, wherein the predetermined time is a number of clock cycles of a free-running clock of the integrated circuit.
4. The method of claim 1 wherein, the reducing of the high frequency clocking of circuitry gradually to zero includes
 - clocking circuitry at a first frequency, and,
 - before clocking the circuitry at a second frequency lower than the first frequency,
 - waiting a predetermined time during the clocking of the circuitry at the first frequency.

1 5. The method of claim 1, wherein,
2 after starting the clocking of the circuitry at the
3 low frequency, the method further includes
4 gradually increasing the frequency of the
5 clocking of the circuitry to the high frequency.

1 6. The method of claim 5 wherein,
2 the gradual increasing of the frequency of the
3 clocking of circuitry to the high frequency includes
4 clocking circuitry at a first frequency, and,
5 before clocking the circuitry at a second
6 frequency higher than the first frequency,
7 waiting a predetermined time during the clocking
8 of the circuitry at the first frequency.

1 7. The method of claim 1, wherein,
2 global functional activity in the integrated circuit
3 is proportional to temperature of the integrated circuit
4 and
5 the predetermined limit of global functional activity
6 is proportional to an expected temperature level of the
7 integrated circuit.

1 8. The method of claim 1, wherein
2 the reducing of the high frequency clocking of the
3 circuitry gradually to zero avoids large variations in
4 current otherwise associated with a rapid shut-off of the
5 clocking of circuitry.

1 9. The method of claim 5, wherein
2 the starting of the clocking of the circuitry at the
3 low frequency and the gradual increase in the frequency of
4 the clocking of the circuitry to the high frequency avoids

5 large variations in current otherwise associated with a
6 rapid turn-on of the clocking of circuitry.

1 10. An integrated circuit comprising:
2 a clock generator to generate a clock;
3 an activity detector to measure global functional
4 activity of the integrated circuit; and
5 a clock throttling controller coupled to the activity
6 detector and the clock generator, the clock throttling
7 controller to generate a throttled clock to couple to
8 functional blocks of the integrated circuit for clocking
9 circuitry therein, the clock throttling controller to
10 gradually throttle the frequency of the throttled clock to
11 the functional blocks in response to the measure of the
12 global functional activity meeting or exceeding a
13 predetermined limit.

1 11. The integrated circuit of claim 10, wherein,
2 the activity detector receives measures of local
3 functional activity associated with each functional block
4 of the integrated circuit to measure the global functional
5 activity of the integrated circuit.

1 12. The integrated circuit of claim 10, wherein,
2 the activity detector receives measures of local
3 functional activity associated with each functional block
4 of the integrated circuit to determine the measure of the
5 global functional activity of the integrated circuit,
6 the activity detector compares the measure of the
7 global functional activity with the predetermined limit to
8 determine if it is met or exceeded, and
9 the activity detector signals to the clock throttling
10 controller whether or not the predetermined limit has been
11 met or exceeded.

1 13. The integrated circuit of claim 10, further
2 comprising,
3 a logical gate coupled to the clock generator to
4 receive the clock and the clock throttling controller to
5 receive a control signal, the logical gate to periodically
6 mask out one or more clock cycles of the clock to generate
7 the throttled clock in response to the control signal to
8 gradually throttle the frequency of the throttled clock.

1 14. The integrated circuit of claim 13, wherein,
2 the logical gate is an AND gate to logically AND the
3 clock and the control signal from the clock throttling
4 controller together.

1 15. The integrated circuit of claim 10, wherein,
2 one hundred percent of the circuitry in the
3 functional blocks can have the throttled clock stopped.

1 16. The integrated circuit of claim 10, wherein,
2 less than one hundred percent of the circuitry in the
3 functional blocks can have the throttled clock stopped.

1 17. The integrated circuit of claim 16, wherein,
2 only the circuitry to which the throttled clock can
3 be stopped is the throttled clock coupled and its
4 frequency gradually throttled in response to the measure
5 of the functional activity meeting or exceeding the
6 predetermined limit.

1 18. The integrated circuit of claim 10, wherein,
2 the frequency of the throttled clock is gradually
3 throttled OFF and then ON in response to the measure of
4 the functional activity meeting or exceeding the
5 predetermined limit.

1 19. A clock generator comprising:
2 a free-running clock generator to generate a free-
3 running clock;
4 a thermal activity detector to generate a total
5 measure of functional activity in an integrated circuit
6 and to determine whether or not the total measure of
7 functional activity meets or exceeds a thermal limit of
8 activity to generate an enable thermal throttling signal;
9 and
10 a clock throttling controller coupled to the thermal
11 activity detector and the free-running clock generator,
12 the clock throttling controller to generate a throttled
13 clock to couple to functional blocks of the integrated
14 circuit for clocking circuitry therein, the clock
15 throttling controller to gradually throttle the frequency
16 of the throttled clock to circuitry of the functional
17 blocks in response to the enable thermal throttling
18 signal.

1 20. The clock generator of claim 19, wherein,
2 the clock throttling controller includes,
3 a linear feedback shift register connected in a loop
4 to generate a clock gating control signal, the clock
5 gating control signal to selectively mask out clock cycles
6 in the throttled clock to gradually reduce its frequency
7 and to selectively insert clock cycles into the throttled
8 clock to gradually increase its frequency, and
9 a state machine coupled to the linear feedback shift
10 register to control the selective masking out of clock
11 cycles and the selective inserting of clock cycles in the
12 throttled clock to gradually throttle the frequency down
13 to shut OFF the throttled clock and gradually throttle the

